TRANSMITTAL FORM

Attorney Docket No.
RAL9-99-0056/1474P

AF/2123

In re the application **BULLIS, et al.**

Serial No: **09/409,940**

Filed: **September 30, 1999**

Confirmation No: **6159**

Group Art Unit: **2123**

Examiner: **Ferris III, F.**

For: **METHOD AND SYSTEM FOR PROVIDING HIERARCHICAL SELF-CHECKING IN ASIC SIMULATION**

ENCLOSURES *(check all that apply)*		
☐ Amendment/Reply	☐ Assignment and Recordation Cover Sheet	☐ After Allowance Communication to Group
☐ After Final	☐ Part B-Issue Fee Transmittal	☐ Appeal Communication to Board of Appeals and Interferences
☐ Information disclosure statement	☐ Letter to Draftsman	■ Reply Brief *(in triplicate)*
☐ Form 1449	☐ Drawings	☐ Status Letter
☐ (X) Copies of References	☐ Petition	■ Postcard
☐ Extension of Time Request *	☐ Fee Address Indication Form	☐ Other Enclosure(s) *(please identify below)*:
☐ Express Abandonment	☐ Terminal Disclaimer	
☐ Certified Copy of Priority Doc	☐ Power of Attorney and Revocation of Prior Powers	
☐ Response to Incomplete Appln	☐ Change of Correspondence Address	
☐ Response to Missing Parts	*Extension of Term: Pursuant to 37 CFR 1.136, Applicant petitions the Commissioner to extend the time for response for xxxxxx month(s), from to .	
☐ Executed Declaration by Inventor(s)		

CLAIMS					
FOR	Claims Remaining After Amendment	Highest # of Claims Previously Paid For	Extra Claims	RATE	FEE
Total Claims	0	0	0	$18.00	$ 0.00
Independent Claims	0	0	0	$86.00	$ 0.00
				Total Fees	$ 0.00

METHOD OF PAYMENT

☐	Check no. _____ in the amount of $ _____ is enclosed for payment of fees.
■	Charge $ 330.00 to Deposit Account No. 50-0563 (IBM Corp.) for payment of fees.
■	Charge any additional fees or credit any overpayment to Deposit Account No. 50-0563 (IBM Corp.)

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Attorney Name	Joseph A. Sawyer, Jr., Reg. No. 30,801
Signature	
Date	December 22, 2003

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this date: December 22, 2003

Type or printed name	Grace Alicea
Signature	

#16 Reply
1-13-04

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

APPEAL NO:

In Re Application of:

Date: December 22, 2003

Bullis et al.

Serial No. 09/409,940

Group Art Unit: 2123

Filed: September 30, 1999

Examiner: Ferris III, F.

For: METHOD AND SYSTEM FOR PROVIDING HIERARCHICAL SELF-CHECKING IN ASIC SIMULATION

APPELLANT'S REPLY TO EXAMINER'S ANSWER

Attorney for Appellants
International Business Machines Corp.
Sawyer Law Group LLP

01/02/2004 CNGUYEN 00000084 500563 09409940
01 FC:1402 330.00 DA

TOPICAL INDEX

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

APPEAL NO:

In Re Application of: Date: December 22, 2003

Bullis et al.

Serial No. 09/409,940 Group Art Unit: 2123

Filed: September 30, 1999 Examiner: Ferris III, F.

For: METHOD AND SYSTEM FOR PROVIDING HIERARCHICAL SELF-CHECKING IN ASIC SIMULATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPELLANT'S REPLY TO EXAMINER'S ANSWER

Sir:

Appellant herein files a Reply to the Examiner's Answer as follows:

I. STATUS OF AMENDMENT

Appellant agrees that the final amendment and declaration had not been entered and that the Examiner indicated that the Examiner found "the declaration merely expresses the opinion of the inventor, is not supported by sufficient evidence, and is in variance with the Inventor's previously filed declaration."

II. ISSUES

The issues presented are:

(1) whether claims 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, and 23 are each unpatentable under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains; and

(2) 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, and 23 are each unpatentable under 35 U.S.C. § 103 as being obvious in light of U.S. Patent No. 6,182,258 (Hollander) in view of U.S. Patent No. 6,006,024 (Guruswamy).

III. ARGUMENTS

A. Summary of the Applied Rejections

In the Final Office Action, dated February 20, 2003, the Examiner rejected claims 1-23 under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains. With respect to claim 1, the Examiner cited the use of the terms "snooper," "interface," "checker," and "generator." The Examiner also objected to the Second Declaration. The Examiner's rejection under 35 U.S.C. § 112, first paragraph is further described in Appellant's Brief filed on September 23, 2003.

The Examiner further rejected claims 1-23 under 35 U.S.C. § 103 as being unpatentable over Hollander in view of Guruswamy. The Examiner's rejection under 35 U.S.C. § 103 is further described in Appellant's Brief filed on September 23, 2003.

Appellant respectfully requests that the Board reverse the Examiner's final rejection of claims 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, and 23 under 35 U.S.C. § 112, first paragraph, and the Examiner's final rejection of claims 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, and 23 under 35 U.S.C. § 103.

B. The Cited Prior Art

The cited prior art is described in Appellant's Brief filed on September 23, 2003.

C. Claims 1-23 Are Not Unpatentable Under 35 U.S.C. § 112, First Paragraph.

Appellant respectfully submits that the applied rejections of claims 1-23 under 35 U.S.C. § 112, first paragraph, are without merit as the Examiner has completely failed to explain why the specification fails to describe, in such a way as to enable one skilled in the art to which it pertains or with which it is most nearly connected, to make and/or use the invention, the subject matter of the claims. In particular, the Examiner objected to the use of the terms "snooper," "interface," "checker," and "generator." In the Examiner's Answer, the Examiner indicated that if "the 'snooper' is realized in software, then an algorithm and flow chart of the 'snooping' process should be disclosed. If the 'snooper' is realized in hardware, then a block diagram and the hardware description should be provided." Examiner's Answer, page 7, 18-20. With respect to the term "interface" the Examiner indicated that "the applicants have not identified a standard interface nor have they disclosed one of their own design. The specifics of the claimed 'interface' appear to be critical matter relating to the operation of the claimed invention and needs to be disclosed in detail." Examiner's Answer, page 8, lines 1-4. The Examiner also indicated that the issue with the checker is that the specification "does not disclose how the checker performs the claimed 'checking' of the output and does not disclose what constitutes a 'desired output'." Examiner's Answer, page 8, lines 8-10. The Examiner also indicated that with respect to the generator, "no description of the interface coupling [for the generator] or the related inputs and outputs is provided. Further, no description or explanation of how the generator is 'directed by a test case' is given and there is no description of how the generator actually functions." Examiner's Answer, page 8, lines 14-17. The

Examiner further stated that the Second Declaration, to which the Examiner objected, was in variance with the previously filed First Declaration and that the First Declaration buttresses the Examiner's position. Examiner's Answer, page 4, lines 20-21 and page 5, lines 7-8.

Appellant respectfully disagrees with the Examiner. Appellant respectfully stands by the arguments regarding this issue and that can be found in Appellants Brief, filed on September 23, 2004. In particular, Appellant respectfully submits that the snooper, checker, generator, interface, and test case, particularly when including new Figures 7A-7C and the accompanying discussion as well as the Second Declaration, are described by the specification in such a way as to enable one skilled in the art to which it pertains or with which it is most nearly connected, to make and/or use the invention, the subject matter of the claims.

Further, when taking into account the knowledge of one of ordinary skill in the art with respect to conventional test cases and models, the specification describes, in such a way as to enable one skilled in the art to which it pertains or with which it is most nearly connected, to make and/or use the invention, the subject matter of the claims. As described in the specification, conventional test cases are used to test individual islands and, once groups of islands are integrated, to test groups of islands. Specification, page 2, lines 21-22 and page 3, lines 10-15. For example, Figures 2B, 2C, and 2D depict the use of various conventional test cases and models at different levels in a hierarchically designed integrated circuit. As stated in the specification, the conventional test cases and the accompanying models are typically used in the simulation stage of integrated circuit design. Specification, page 1, lines 14-18 and page 2, lines 14-15. Consequently, Appellant respectfully submits that one of ordinary skill in the art would be familiar with conventional test cases and would understand how conventional test cases are coupled to islands or groups of islands, as well as how conventional test cases function

in general.

Although conventional test cases and their corresponding conventional models can be used to test integrated circuits, one of ordinary skill in the art will also understand that there are issues in using conventional test cases. In particular, a new set of test cases and models is provided for each level of the hierarchy, resulting in an extremely large number of test cases and models as well as consuming a significant amount of resources. Specification, page 6, lines 14-22.

The method, system, and computer-readable medium recited in claims 1-23 remedy the defects of the conventional test cases and model combination. In particular, the Specification states that "the snooper 102, checker 104 and generator 106 can *replace the conventional model* in checking the I[ntegrated]C[ircuit]." Specification, page 13, line 23-page 14, line 1 (emphasis added). Thus, although the functions provided by the snooper, checker and generator differ from the model, their locations in the testing are analogous to the conventional model. Compare Figure 4A with Figure 2B. The recited test case is also analogous to the conventional test cases, but are simpler and fewer are required to exhaustively test islands in an integrated circuit. Specification, page 13, lines 4-5. The recited snooper, checker, and generator in combination with the recited test case can be viewed as replacing the conventional model and conventional test case combination. Consequently, Appellant respectfully submits that one of ordinary skill in the art would understand how to couple the snooper, checker, and generator to islands in the integrated circuit. Stated differently, one of ordinary skill in the art would understand how the conventional model and test case are coupled to the integrated circuit. Consequently, one of ordinary skill in the art would also understand how to couple the recited snooper, checker, and generator to the integrated circuit. In other words, one of ordinary skill in the art would

understand the term "interface" to which the snooper, checker, and generator are coupled, as recited in the claims

> Furthermore, the specification further states that the
>
> test case 107 is preferably composed of routines which provide varying degrees of control to the generator 106. The generator 106 responds to the routines to check the IC 10 in conjunction with the snooper 102 and checker 104. The test case 107 can be provided using a number of languages and still function with the snooper 102, checker 104 and generator 106. . . However, the test case 107 is preferably in the same language as the snooper 102, checker 104 and generator 106.

Specification, page 11, lines 11-19. The specification also states:

> [t]he snooper 102, checker 104 and generator 106 are preferably made using the same code as the IC with which the snooper 102, checker 104 and generator 106 are used. Thus, the snooper 102, checker 104 and generator 106 are preferably provided using a behavioral language. However, the IC is often represented in a number of ways. For example, during development, the IC may be represented using the behavioral language, register transfer level ("RTL") and gates. The representation of the IC often changes for different phases of the development of the IC. It is generally desirable to provide a simulation environment for these different representations of the IC. In a preferred embodiment, therefore, use of different representations for the islands in the IC does not affect the operation of the snooper 102, checker 104 and generator 106. Consequently, the snooper 102, checker 104 and generator 106 can be used for checking the IC during multiple phases of development.

Specification, page 11, line 19-page 20, line 7. More specifically with respect to the snooper, the specification states that the snooper preferably "has sufficient intelligence, for example understanding a bus protocol, to determine which data should be obtained from the interface and provide the appropriate data to the interface. Specification, page 12, lines 14-16. Furthermore, Appellant has previously added Figures 7A, 7B, and 7C and the accompanying discussion which indicate the functions of the snooper, checker, and generator. Consequently, Appellant respectfully submits that the terms snooper, checker, generator, and interface are described in such a way as to enable one skilled in the art to which it pertains or with which it is most nearly

connected, to make and/or use the invention, the subject matter of the claims.

Appellant also respectfully submits that the Second Declaration is not at variance with the First Declaration and that both declarations support the proposition that the specification describes in such a way as to enable one skilled in the art to which it pertains or with which it is most nearly connected, to make and/or use the invention that the subject matter of the claims. Both the First Declaration and the Second Declaration state that in the inventor's opinion, one of ordinary skill in the art would be capable of making and/or using the invention that is the subject matter of the claims. See paragraphs 1-9 in the Second Declaration; and paragraphs 1-7 of the First Declaration. Paragraphs 8-15 of the First Declaration simply describe a particular embodiment of the snooper, checker, and generator used in conjunction with a specific integrated circuit. Thus, paragraph 8 of the First Declaration states that "[o]ne embodiment" was applied to a particular chip, a CAD processor chip and that other embodiments could be applied to other integrated circuits. First Declaration, Paragraph 8. Consequently, the description in paragraphs 8-15 in the First Declaration of the CAD processor chip are for exemplary purposes only. Thus, by providing a concrete example, the discussion of the snoopers, checkers, and generators as used in testing islands in the CAD processor chip improves the explanation of the snooper, checker, generator, and test cases. However, Appellant respectfully submits that the particular implementation for the particular integrated circuit described in Paragraphs 8-15 of the First Declaration is not necessary to enable one skilled in the art to which it pertains or with which it is most nearly connected, to make and/or use the invention that the subject matter of the claims. Instead, the description of the particular implementation in the First Declaration merely adds to, but is not in variance with the description in the Second Declaration.

Consequently, for the above described reasons, Appellant respectfully submits that the

terms in independent claims 1, 10, and 17 are described in the specification in such a way as to enable one skilled in the art to which it pertains or with which it is most nearly connected, to make and/or use the invention, the subject matter of the claims.

Claims 2, 3, 4, 5, 6, 7, 8, and 9 depend upon independent claim 1. Claims 11, 12, 13, 14, 15, and 16 depend upon independent claim 10. Claims 17, 18, 19, 20, 21, 22, and 23 depend on independent claim 17. Consequently, claims 2-9, 11-16, and 18-23 are allowable for the same reasons discussed above with respect to claims 1, 10, and 17.

Accordingly Appellant respectfully requests that the Board reverse the final rejection of claims 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, and 23 under 35 U.S.C. § 112.

D. Claims 1-23 Are Not Unpatentable Under 35 U.S.C. § 103.

Appellant respectfully submits that the applied rejections of claims 1-23 under 35 U.S.C. § 102(e) as being unpatentable over Hollander in view of Guruswamy are without merit. In particular, the Examiner has completely failed to explain why Hollander in view of Guruswamy teaches or suggests the system, method, and computer-readable medium recited in claims 1, 10, and 17, respectively. Further, the Examiner has failed to explain why Hollander in view of Guruswamy teaches or suggest the systems, methods, and computer-readable media recited in claims 2-9, 11-16, and 18-23, respectively.

Appellant respectfully stands by the arguments in Appellant's Brief, filed on September, 23, 2003 and respectfully draws the Board's attention to the discussion contained therein. In particular, Appellant respectfully disagrees that the cited references describe the recited combination of the snooper, checker, and generator and in which the checker can both generate desired outputs and

check the outputs from the island under test against the desired inputs. In particular, the cited references fail to teach or suggest the recited checker that can both generate desired outputs and check the outputs from the island under test against the desired inputs.

In the Examiner's Answer, the Examiner indicated that Appellant argues that Hollander teaches synchronizing and does not teach synchronizing. Appellant respectfully disagrees with the Examiner. Appellant agrees that Hollander teaches synchronizing the checking module. However, Appellant disagrees that this synchronizing is synonymous with using the checker to both generate desired outputs and check the outputs from the island under test against the desired inputs. Instead, the cited portions of Hollander merely describe the checking and synchronization performed using the checking module of Hollander. It is quite possible that the checking module receives the desired outputs from the test generation module. Thus, even if the system of Hollander responds to the outputs of the device under test, Appellant can find no indication that it is the checking module, not the test generation module or some other module, that determines the desired outputs. Consequently, Hollander fails to teach or suggest the recited system, method, and computer-readable medium in which the checker both generates the desired inputs and checks the actual inputs against the desired inputs

Guruswamy fails to remedy the defects of Hollander. Although Guruswamy does describe dividing an IC into islands, Appellant can find no mention in the cited portions of Guruswamy of using a checker to not only check the outputs of the island under test, but also to generate the desired outputs based upon the inputs. Thus, if the teachings of Guruswamy are combined with those of Hollander, the combination might use the system of Hollander to check the performance of a circuit laid out in accordance with the teachings of Guruswamy. The combination might even synchronize the checking module with other modules. However, because neither the cited portions

of Hollander nor the cited portions of Guruswamy describe using the checker to both generated the desired outputs based on the inputs and check the outputs against these desired outputs, any combination of Hollander and Guruswamy would also omit this feature. Hollander in view of Guruswamy thus fail to teach or suggest a system, method, or computer-readable medium that includes a checker that generates desired output based upon the inputs to the island and checks the actual outputs against the desired outputs. Accordingly, Appellant respectfully submits that independent claims 1, 10 and 17 are allowable over the cited references.

Claims 2, 3, 4, 5, 6, 7, 8, and 9 depend upon independent claim 1. Claims 11, 12, 13, 14, 15, and 16 depend upon independent claim 10. Claims 17, 18, 19, 20, 21, 22, and 23 depend on independent claim 17. Consequently, claims 2-9, 11-16, and 18-23 are allowable for the same reasons discussed above with respect to claims 1, 10, and 17.

Accordingly Appellant respectfully requests that the Board reverse the final rejection of claims 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, and 23 under 35 U.S.C. § 103.

E. Summary of Arguments

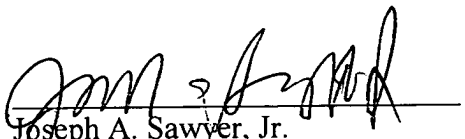
For all the foregoing reasons, it is respectfully submitted that Claims 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, and 23 (all the claims presently in the application) are patentable for defining subject matter which would not have been obvious under 35 U.S.C. § 103 or and contain only subject matter described in the specification in a manner which comports with the requirements of 35 U.S.C. § 112, first paragraph. Thus, Appellant respectfully requests that the Board reverse the rejection of all the appealed Claims and find each of these Claims allowable.

Note: For convenience of detachment without disturbing the integrity of the remainder of pages of this Reply, an "APPENDIX" section is contained on separate sheets following the signatory portion of this Reply.

This Reply is being submitted in triplicate, and authorization for payment of the required Reply fee is contained in the cover letter for this Reply. Please charge any fee that may be necessary for the continued pendency of this application to Deposit Acct. 50-0563 (IBM Corp.)

Very truly yours,

December 22, 2003



Joseph A. Sawyer, Jr.
Attorney for Appellants
Reg. No. 30,801
(650) 493-4540

IV. APPENDIX

1. A system for providing simulation of an integrated circuit during development of the integrated circuit, the integrated circuit having an island including an interface, the system comprising:

a snooper coupled with the interface for monitoring the interface and obtaining an output provided by the island during simulation;

a checker, coupled with the interface, for checking the output to determine whether the output is a desired output;

a generator coupled with the island for providing an input to the island during simulation; and

at least one test case coupled with the generator for directing the generator;

wherein the checker further determines the desired output based upon the input; and

wherein the generator further includes intelligence to provide the input to the island based only upon data and a request provided by the at least one test case to the generator, the request requesting that the generator perform a particular simulation on the island.

2. The system of claim 1 wherein the checker is coupled with the snooper and wherein the checker receives the output from the snooper.

3. The system of claim 1 wherein the snooper may be reused when the island is integrated with a second island.

4. The system of claim 1 wherein the checker may be reused when the island is

integrated with a second island.

5. The system of claim 1 wherein the generator may be reused when the island is integrated with a second island.

6. The system of claim 1 wherein the generator receives the output and provides the input based on the output.

7. The system of claim 1 wherein the generator and the snooper are coupled with the interface, wherein the checker is coupled with the interface through the snooper and wherein only the snooper and the checker are reused when a second island is integrated with the island at the interface.

8. The system of claim 1 wherein the at least one test case further provides data and instructions to the generator.

9. The system of claim 1 wherein the interface is an internal interface.

10. A method for providing simulation of an integrated circuit during development of the integrated circuit, the integrated circuit having an island including an interface, the method comprising the steps of:

(a) monitoring the interface to obtain an output provided by the island during simulation;

(b) checking the output to determine whether the output is a desired output, the checking step (b) further including the step of

(b1) determining the desired output based upon an input;

(c) providing the input to the island during simulation; and

(d) directing the providing of the input using at least one test case;

wherein the input is provided to the island using a generator including intelligence to provide the input to the island based only upon data and a request provided by the at least one test case to the generator, the request requesting that the generator perform a particular simulation on the island.

11. The method of claim 10 wherein step (a) further includes the step of:

(a1) snooping the interface to obtain the output provided by the island during simulation using a snooper, the snooper capable of being reused when the island is integrated with a second island.

12. The method of claim 10 wherein step (b) further includes the step of:

(b1) checking the output using a checker to determine whether the output is the desired output, the checker capable of being reused when the island is integrated with a second island.

13. The method of claim 10 wherein step (c) further includes the step of:

(c1) providing the input to the island during simulation using a generator, the generator capable of being reused when the island is integrated with a second island.

14. The method of claim 10 wherein step (c) further includes the step of:

(c1) providing an input to the island during simulation using a generator, the generator receiving the output and providing the input based on the output.

15. The method of claim 14 wherein the directing step (d) further includes the step of:

(d1) providing data and instructions from the at least one test case to the generator.

16. The method of claim 10 wherein the interface is an internal interface.

17. A computer-readable medium having a program for providing simulation of an integrated circuit during development of the integrated circuit, the integrated circuit having an island including an interface, the program comprising instructions for:

(a) monitoring the interface to obtain an output provided by the island during simulation;

(b) checking the output to determine whether the output is a desired output, the checking step (b) further including the step of

(b1) determining the desired output based upon an input;

(c) providing the input to the island during simulation; and

(d) directing the providing of the input using at least one test case;

wherein the input is provided to the island using a generator including intelligence to provide the input to the island based only upon data and a request provided by the at least one test case to the generator, the request requesting that the generator perform a particular simulation on the island.

18. The computer-readable medium of claim 17 wherein the instruction for snooping (a) further includes the instructions for:

(a1) snooping the interface to obtain the output provided by the island during simulation using a snooper, the snooper capable of being reused when the island is integrated with a second island.

19. The computer-readable medium of claim 17 wherein the instruction for checking (b) further includes instructions for:

(b1) checking the output using a checker to determine whether the output is the desired output, the checker capable of being reused when the island is integrated with a second island.

20. The computer-readable medium of claim 17 wherein the input providing step (c) further includes instructions for:

(c1) providing the input to the island during simulation using a generator, the generator capable of being reused when the island is integrated with a second island.

21. The computer-readable medium of claim 17 wherein the input providing step (c) further includes instructions for:

(c1) providing an input to the island during simulation using a generator, the generator receiving the output and providing the input based on the output.

22. The computer-readable medium of claim 17 wherein the directing instructions (d)

further includes the instructions for:

(d1) providing data and instructions from the at least one test case to the generator.

23. The computer-readable medium of claim 17 wherein the interface is an internal interface.